Amendments to the Claims

This listing of the claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (currently amended): A semiconductor structure comprising:

an emitter mesa containing at least one layer;

a base layer;

an emitter ledge layer located above the base layer and below the emitter mesa, the emitter ledge layer having an intrinsic region located beneath the emitter mesa and an extrinsic region located outside the intrinsic region, the extrinsic region comprising depleted semiconductor material, wherein the emitter ledge layer is composed of a ledge layer material different from a material of the at least one layer; and

one or more base contacts formed within a portion of the extrinsic region of the emitter ledge layer and spaced at selected distances from the emitter mesa,

wherein the one or more base contacts electrically contact the base layer, and wherein the base contacts and the emitter ledge layer are disposed to cover an upper surface of the base layer so that there are no gaps in the emitter ledge layer between the one or more base contacts and the emitter mesa to leave the upper surface of the base layer exposed.

2. (original): The semiconductor structure of claim 1, wherein the extrinsic region of the emitter ledge layer comprises fully depleted semiconductor material.

3. (original): The semiconductor structure of claim 1, wherein the semiconductor structure comprises a portion of a heterojunction bipolar transistor (HBT).

4. (original): The semiconductor structure of claim 3, wherein the HBT comprises an InP-based NPN HBT.

5. (original): The semiconductor structure of claim 4, wherein the emitter mesa comprises:

an emitter cap layer comprising layers of n^+ InGaAs and n^+ AlInAs, and an emitter layer comprising n^- AlInAs.

6. (original): The semiconductor structure of claim 4, wherein the emitter mesa comprises:

an emitter cap layer comprising layers of n^+ InGaAs and n^+ InP;

an emitter layer comprising n^- InP; and,

an etch stop layer comprising AlGaInAs.

7. (original): The semiconductor structure of claim 4, wherein the InP-based HBT comprises a single heterojunction bipolar transistor or a double heterojunction bipolar transistor.

8. (original): The semiconductor structure of claim 1, wherein the emitter mesa is formed by etching down to the emitter ledge layer after an emitter contact is formed on the emitter mesa.

9. (original): The semiconductor structure of claim 8, wherein one or more portions of the extrinsic region of the emitter ledge layer are etched down to the base region to open one or more areas for the one or more base contacts and the one or more base contacts are formed by depositing metal in the one or more areas.

10. (original): The semiconductor structure of claim 9, wherein the one or more base contacts further comprise metal deposited on top of one or more portions of the emitter ledge layer, said metal deposited on top of the one or more portions of the emitter ledge layer in electrical contact with the metal deposited in the one or more areas.

11. (original): The semiconductor structure of claim 1, wherein the extrinsic region of the emitter edge layer serves as a surface passivation layer for an upper surface of the base

layer.

12. (original): The semiconductor structure of claim 1, wherein the emitter ledge layer comprises n^- InP.

13-25 (canceled)

26. (currently amended): A semiconductor structure comprising an InP-based NPN heterojunction bipolar transistor (HBT) wherein the InP-based NPN HBT has a fully depleted emitter ledge layer region disposed between one or more base contacts and an emitter mesa to 100% or nearly 100% passivate an upper surface of a base layer of the InP-based NPN HBT, wherein the emitter mesa comprises at least one layer that is composed of different material than the emitter ledge layer.

27. (original): The semiconductor structure of claim 26, wherein the fully depleted emitter ledge layer region has no gaps in the emitter ledge layer between the one or more base contacts and the emitter mesa to leave an upper surface of the base layer exposed.

28. (new): A semiconductor structure comprising:

an emitter mesa;

a base layer;

an emitter ledge layer located above the base layer and below the emitter mesa, the emitter ledge layer having an intrinsic region located beneath the emitter mesa and separated from the emitter mesa by an etch stop layer and an extrinsic region located outside the intrinsic region, the extrinsic region comprising depleted semiconductor material; and

one or more base contacts formed within a portion of the extrinsic region of the emitter ledge layer and spaced at selected distances from the emitter mesa,

wherein the one or more base contacts electrically contact the base layer, and wherein the base contacts and the emitter ledge layer are disposed to cover an upper surface of the base layer so that there are no gaps in the emitter ledge layer between the

one or more base contacts and the emitter mesa to leave the upper surface of the base layer exposed.

29. (new): A semiconductor structure comprising an InP-based NPN heterojunction bipolar transistor (HBT) wherein the InP-based NPN HBT has a fully depleted emitter ledge layer region disposed between one or more base contacts and an emitter mesa to 100% or nearly 100% passivate an upper surface of a base layer of the InP-based NPN HBT, wherein the emitter ledge layer is separated from the emitter mesa by an etch stop layer.